What is claimed is:

CLAIMS

1. An apparatus suitable for simulating a standard wafer in semiconductor manufacturing equipment, comprising:

a support layer suitable for being handled by the semiconductor manufacturing equipment; and

a mixture including a process agent and a material, the mixture being applied to the support layer,

wherein the apparatus simulates a wafer including the material and having the process agent thereon.

2. The apparatus of claim 1, wherein the process agent is photoresist.

3. The apparatus of claim 1, wherein the material is silicon and the apparatus simulates a wafer including polysilicon.

4. The apparatus of claim 1, wherein the material is tungsten and the apparatus simulates a wafer including tungsten.

5. The apparatus of claim 1, wherein the material is tungsten silicide and the apparatus simulates a wafer including tungsten silicide.

6. The apparatus of claim 1, wherein the material is titanium and the apparatus simulates a wafer including titanium.

7. The apparatus of claim 1, wherein the material is titanium nitride and the apparatus simulates a wafer including titanium nitride.

8. The apparatus of claim 1, wherein the material is silicon dioxide and the apparatus simulates a wafer including silicon dioxide.

9. The apparatus of claim 1, wherein the material is aluminum and the apparatus simulates a wafer including aluminum.

10. The apparatus of claim 1, wherein the material is platinum and the apparatus simulates a wafer including platinum.

11. The apparatus of claim 1, wherein the material is ruthenium and the apparatus simulates a wafer including ruthenium.

12. The apparatus of claim 1, wherein the material is ruthenium oxide and the apparatus simulates a wafer including ruthenium oxide.

13. The apparatus of claim 1, wherein the material is copper and the apparatus simulates a wafer including copper.

14. The apparatus of claim 1, wherein the material is tantalum and the apparatus simulates a wafer including tantalum.

15. The apparatus of claim 1, wherein the material is nickel and the apparatus simulates a wafer including nickel.

16. The apparatus of claim 1, wherein the support layer is at least one of a disc and a wafer.

17. The apparatus of claim 1, wherein the support layer includes at least one of silicon, metal, plastic, and an oxide.

18. The apparatus of claim 1, wherein the material and the process agent of the mixture are baked on the support layer.

19. The apparatus of claim 1, wherein a ratio between the material to the process agent corresponds to an exposed area on the wafer to be simulated.

20. A process for manufacturing an apparatus suitable for use in simulating a standard wafer in semiconductor manufacturing equipment, comprising:

combining a process agent and a material; and

applying the combination of the process agent and the material to a support layer to simulate a wafer including the material and having the process agent thereon.

21. The process of claim 20, wherein the process agent is a photoresist.

22. The process of claim 20, wherein the material is silicon dioxide to simulate a wafer including polysilicon.

23. The process of claim 20, wherein the material is tungsten to simulate a wafer including tungsten.

24. The process of claim 20, wherein the material is tungsten silicide to simulate a wafer including tungsten silicide.

25. The process of claim 20, wherein the material is titanium to simulate a wafer including titanium.

26. The process of claim 20, wherein the material is titanium nitride to simulate a wafer including titanium nitride.

27. The process of claim 20, wherein the material is silicon dioxide to simulate a wafer including silicon dioxide.

28. The process of claim 20, wherein the material is aluminum to simulate a wafer including aluminum.

29. The process of claim 20, wherein the material is platinum to simulate a wafer including platinum.

30. The process of claim 20, wherein the material is ruthenium to simulate a wafer including ruthenium.

31. The process of claim 20, wherein the material is ruthenium oxide to simulate a wafer including ruthenium oxide.

32. The process of claim 20, wherein the material is copper to simulate a wafer including copper.

33. The process of claim 20, wherein the material is tantalum to simulate a wafer including tantalum.

34. The process of claim 20, wherein the material is nickel to simulate a wafer including nickel.

35. The process of claim 20, wherein the support layer is at least one of a disc and a wafer.

36. The process of claim 20, wherein the support layer includes at least one of silicon, metal, plastic, and an oxide.

37. The process of claim 20, comprising:

baking the combination of the material and the process agent onto the support layer.

38. The process of claim 20, comprising:

selecting a ratio between the material and the process agent that corresponds to an exposed area on the wafer to be simulated.

39. The process of claim 38, comprising:

mixing the process agent and the material such that the combination is a mixture.

40. In a semiconductor plasma chamber, a method for simulating a standard wafer using an apparatus composed of a combination of a process agent and a material applied to a support layer, the method comprising:

placing the apparatus within the semiconductor plasma chamber;

etching the apparatus; and

simulating the standard wafer by simultaneously producing byproducts during the etching that are similar to byproducts produced by the standard wafer.

41. The method of claim 40, wherein the process agent is photoresist.

42. The method of claim 40, wherein the material is silicon dioxide to simulate a wafer including polysilicon.

43. The method of claim 40, wherein the material is tungsten to simulate a wafer including tungsten.

44. The method of claim 40, wherein the material is tungsten silicide to simulate a wafer including tungsten silicide.

45. The method of claim 40, wherein the material is titanium to simulate a wafer including titanium.

46. The method of claim 40, wherein the material is titanium nitride to simulate a wafer including titanium nitride.

47. The method of claim 40, wherein the material is silicon dioxide to simulate a wafer including silicon dioxide.

48. The method of claim 40, wherein the material is aluminum to simulate a wafer including aluminum.

49. The method of claim 40, wherein the material is platinum to simulate a wafer including platinum.

50. The method of claim 40, wherein the material is ruthenium to simulate a wafer including ruthenium.

51. The method of claim 40, wherein the material is ruthenium oxide to simulate a wafer including ruthenium oxide.

52. The method of claim 40, wherein the material is copper to simulate a wafer including copper.

53. The method of claim 40, wherein the material is tantalum to simulate a wafer including tantalum.

54. The method of claim 40, wherein the material is nickel to simulate a wafer including nickel.

55. The method of claim 40, wherein the support layer is at least one of a disc and a wafer.

56. The method of claim 40, wherein the support layer includes at least one of silicon, metal, plastic, and an oxide.

57. The method of claim 40, wherein the material and the process agent are baked on the support layer.

58. The method of claim 40, wherein a ratio between the material and the process agent corresponds to an exposed area on the wafer to be simulated.

59. An apparatus suitable for simulating a standard manufactured device in manufacturing equipment, comprising:

a support layer suitable for being handled by the manufacturing equipment; and

a mixture including a process agent and a material, the mixture being applied to the support layer,

wherein the apparatus simulates a manufactured device including the material and having the process agent thereon.